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The control and measurement of high power high-gradient acceleration structures*

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Conditioning an accelerating structure is important, and its performance is limited by breakdown and vacuum degradation, hence the necessity of finding problem in the conditioning. In order to save time, a judging process built in the firmware layer is applied in this paper. The system using the embedded algorithm in the Field Programmable Gate Array (FPGA) locates the position of breakdown and displays the result in the user interface. Also, the system has the functions of automatic conditioning and interlock protection, which are useful during the conditioning process of an S-band accelerating structure.

Keywords: Conditioning, Location of breakdown, Automation and Interlock protection, FPGA

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I. INTRODUCTION

Acceleration structures of high gradient and high repetition rate, and the control and measurement in high-power tests of high-gradient acceleration structures, are important in developing compact linacs [1–3]. The RF systems of linac-testing facilities at CLIC, Spring-8, SNS etc., benefit from the use of automatic control. These controllers are basically implemented in hardware to achieve signal acquisition, and the C, C++, JAVA or other programming language for self-developing software or other software are used in data analysis [4]. But still, it is hard to find a breakdown location in real time. This paper is aimed at implementing the collected data waveforms in field programmable gate arrays (FPGA) to spot a specific breakdown location in real time. This saves time in solving problems of hardware malfunction of a linac. The conditioning process can be terminated soon, with increased safety and accuracy in conditioning the high-gradient accelerating structure.

II. HARDWARE

The PCI eXtensions for Instrumentation (PXI) bus framework including the ICS-572B board and the RF front with LLRF (low level radio frequency) is shown in Fig. 1 [5–7]. It is a virtual instrument released by National Instruments (NI) in 1997, and is suitable for testing acceleration structure [8]. The ICS-572B board is equipped with two ADC (AD6645) sampling frequencies of up to 105 MHz, which can simultaneously sample the input and reflected signals of the acceleration structure. It contains the high-performance of Xilinx Virtex-II FPGA. The amount of logic gates is up to six million, being in full compliance with the design requirements. It includes also a PCI bus interface in specifications meeting PCI2.2 at speed of 66 MHz/64-bit. Thus, the data communication between the underlying hardware and upper software is well achieved. According to the project requirements, two PXI-5122 data acquisition boards in 100 MHz sampling rate are added.

As shown in Fig. 2, the test platform for high-power S-band accelerating structures is mainly composed of a 45 MW klystron and a SLAC accelerating structure [9, 10]. On the ICS-572B, the DAC output signal is of 25.6 MHz. The frequency of downstream RF front-end is 2997.924 MHz, i.e., the amplifier input. The maximum output power of the state amplifier, which provides input signal to the klystron, is about 1000 W. The output and reflected signals of the klystron, together with the input and output signals of the accelerating structure, and the ICT signal, are displayed and stored in the ICS-572B and PXI-5122 boards [11]. The user interface of the experimental platform is LABVIEW, from which we can set experimental data and display the waveforms. Once the reflected power increases suddenly and exceeds the threshold, the output of DAC module will be reduced to zero to protect the klystron from damage. This kind of protection function is also included in the user interface. In addition, the system can automatically record the reflected signal waveform when breakdown happens.

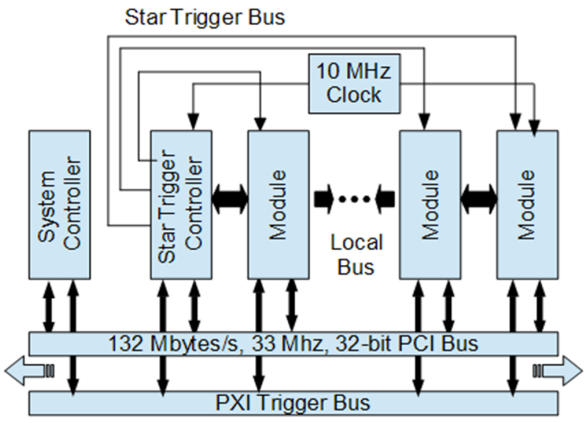

Fig. 1. (Color online) The framework for testing acceleration structure based on PXI.

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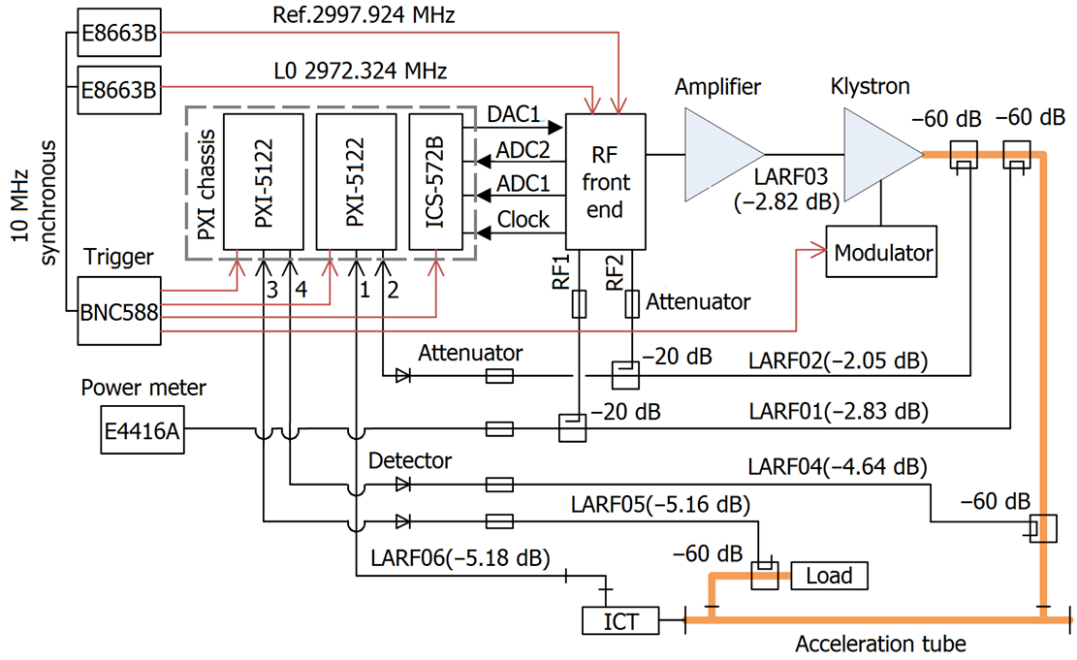

Fig. 2. (Color online) Block diagram of the hardware of the testing platform.

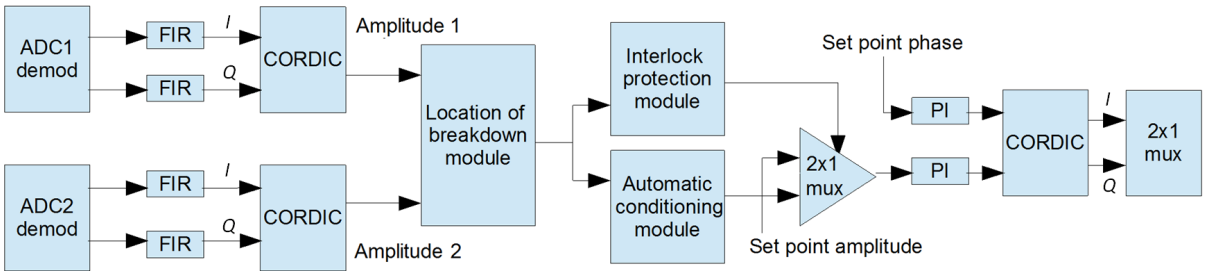

Fig. 3. (Color online) Block diagram of the software of the test platform.

III. SOFTWARE

The software includes three core modules: auto conditioning, interlock protection and breakdown locating. As shown in Fig. 3, I and Q value of the input and reflected signals can be obtained after down-conversion [12], AD sampling and FIR filter. Then, their amplitude can be obtained by using the CORDIC algorithm [13, 14].

A. The automatic conditioning module

Input amplitude of the accelerating structure can be adjusted automatically according to the breakdown numbers in a specified period of time, and the maximum or minimum amplitude of the signal can be imputed manually in the user interface [15]. In the specified period of time, under the threshold of breakdown number, the input amplitude is increased, and decreased otherwise. The variation is limited to the maximum and minimum value set by the system.

B. Interlock protection module

This module detects the power of reflected signal and the vacuum in real time. When the number of breakdown in the accelerating structure exceeds the threshold and the vacuum degrades, the input power of the DAC shall be cut off immediately to protect the system from damage. Figure 4 is the execution procedure of the algorithm [16].

C. The location of breakdown module

The algorithm is based on the difference between the falling edges of the incident and reflected signals to locate the breakdown position [17]. When a breakdown occurs, the subsequent RF signal can hardly pass through the acceleration structure back and forth. The system recognizes the falling edge of the incident and reflected signals inside the FPGA [18], and calculates the time difference (t) by means of the counter.

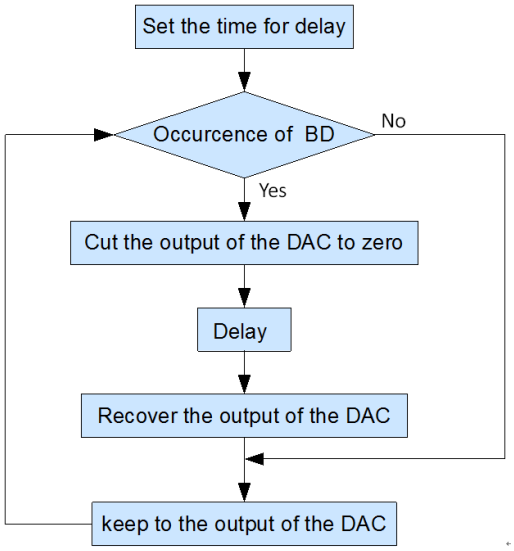

Fig. 4. (Color online) Arithmetic diagram of the interlock protection.

The group velocity equation in the S-band accelerating structure is written as Eq. (1)

$$v_{\mathrm{g}} = (\omega/Q)\left[l - \left(1 - \mathrm{e}^{-2\tau}\right) z\right] /(1 - \mathrm{e}^{-2\tau}), \qquad (1)$$

where, l and Q are total length and quality factor of the acceleration tube, respectively; ω is the frequency; z is the displacement distance from the origin; and τ is the attenuation constant. Let $A = \omega l/[Q(1 - \mathrm{e}^{-2\tau})]$ and $B = \omega/Q$, Eq. (1) can be converted to Eq. (2)

$$z = At/(2 + Bt). \qquad (2)$$

In conditioning an S-band acceleration structure, with given values of z and Q, the group velocity can be calculated easily. Then, using Eq. (2), a lookup table can be made to correspond the relationship between the time when the microwave arrives at each cell and the distance z. So the actual position of breakdown in the accelerating structure can be located against the lookup table, with known value of time (t). Fig. 5 is the principle diagram of the location of breakdown.

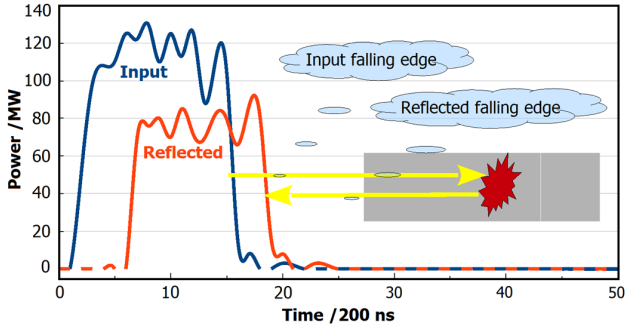

Fig. 5. (Color online) Principle diagram of locating the breakdown position.

IV. THE EXPERIMENT OF CONDITIONING S-BAND ACCELERATION STRUCTURE

The S-band acceleration structure was tested on the platform. In practical operation, the accelerating gradient is supposed to reach 18 MV/m with about 10 Hz petition rate. Before the experiment, it was desirable to provide the klystron with 340 W, 3 μs wide RF excitation signal according to design requirements, and to increase the voltage of the modulator to 5 kV. The width of output pulse of the klystron was set to 0.5 μs by adjusting the output of solid-state amplifier. The voltage was increased by 0.5 kV every 10 min. The vacuum interlock point was set to 1×10^{-5} Pa and the recovery point was 5×10^{-6} Pa. The output and reflected of the klystron, together with the input and output of the accelerating structure were detected by the ICS-572B and PXI-5122.

If the power was conditioned to 20 MW, the modulator output should be decreased to zero. In the experiment, the power could be conditioned to 20 MW at RF pulse width of 0.5, 1.0, 1.5 and 3.0 μs. Figure 6 shows the location of breakdown of these cases.

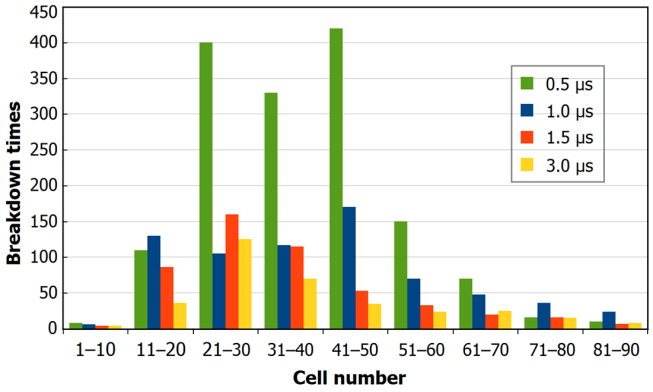

Fig. 6. (Color online) The distribution of location of breakdowns in different cases.

Owing to limited hardware conditions, precision of the system is about four cells length, because the sampling frequency (105 MHz) of the ICS-572B board is not enough to locate the breakdown position to one cell. As we know, the effect of attenuation of the reflected signal along the structure may introduce a bias in the analysis. But in most cases, we can confirm the occurrence of breakdown when amplitude of the reflected signal exceeds the threshold value in spite of the existence of the attenuation.

TABLE 1. Breakdown rate at different output powers (pulse width, 3 μs; trigger frequency, 10 Hz)

Power (MW)	Time (s)	Breakdown rate (e^{-5})
20	64 200	4.67
30	86 400	26.6
36	25 200	158.7

The breakdown rates were monitored at the output powers of 20, 30 and 36 MW . The resulting data are given in Table 1.

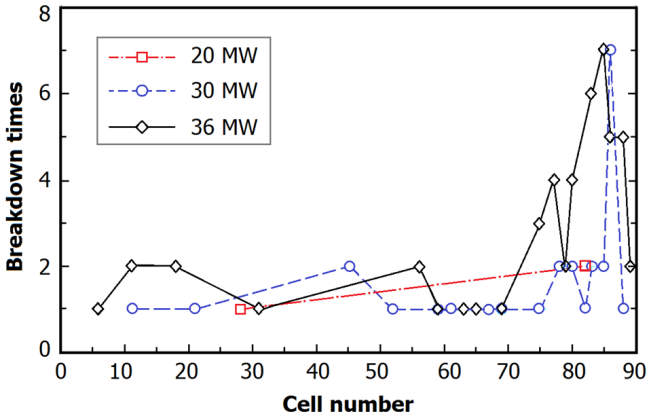

Fig. 7. (Color online) The distribution of breakdowns in breakdown rate testing.

The breakdown rate is higher at output power of 36 MW. According to the breakdown distribution in Fig. 7, most of the breakdowns occurred in cell numbers within 80–90. So we checked up of those cells, and found cell 89 was impaired.

V. CONCLUSION

The testing platform realized the detection of the breakdown position by means of a real-time, fast and accurate field programmable gate array (FPGA). The system not only locates the position of breakdown, but also displays the results in real time. If the breakdowns occur continuously in the same position, it is easy to find the problems and analyze the issues immediately, being of help in protecting the accelerating structures from damage.

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